## L7 Memory System I Cache

1. Why are large memories typically slow?

A) Due to high power consumption

B) Increased density leads to slower access times

C) Larger addressing complexity

D) All of the above

Answer: B) Increased density leads to slower access times

3. Which memory technology requires periodic refreshing?

A) SRAM

B) DRAM

C) Flash

D) Registers

Answer: B) DRAM

4. What principle states that programs tend to access a small portion of memory repeatedly?

A) Memory hierarchy

B) Principle of locality

C) Cache coherence

D) Spatial mapping

Answer: B) Principle of locality

5. In the loop `for (i=0; i<n; i++) sum += a[i];`, which type of locality is exhibited by the array `a[]`?

A) Temporal only

B) Spatial only

C) Both temporal and spatial

D) Neither

Answer: B) Spatial only

6. Which field in a memory address determines the cache set for a direct-mapped cache?

A) Tag

B) Set Index

C) Offset

D) Valid bit

Answer: B) Set Index

7. A cache miss caused by two memory blocks competing for the same cache set is called:

A) Compulsory miss

B) Capacity miss

C) Conflict miss

D) Spatial miss

Answer: C) Conflict miss

8. Which cache organization allows a memory block to be placed in any cache location?

A) Direct-mapped

B) 2-way set associative

C) Fully associative

D) 4-way set associative

Answer: C) Fully associative

9. For a 6-bit address with 2-bit tag, 2-bit index, and 2-bit offset, what is the cache capacity (block size = 4 bytes)?

A) 16 bytes

B) 8 bytes

C) 32 bytes

D) 64 bytes

Answer: A) 16 bytes

10. Increasing cache associativity primarily reduces which type of miss?

A) Compulsory

B) Capacity

C) Conflict

D) Temporal

Answer: C) Conflict

11. Which replacement policy evicts the least recently used block?

A) Random

B) FIFO

C) LRU

D) Round-robin

Answer: C) LRU

12. What is Average Memory Access Time (AMAT) if the hit time is 2 cycles, miss rate is 5%, and miss penalty is 100 cycles?

A) 2 + 0.05\*100 = 7 cycles

B) 2 + 0.95\*100 = 97 cycles

C) 0.05\*100 = 5 cycles

D) 2 + 0.05\*2 = 2.1 cycles

Answer: A) 2 + 0.05\*100 = 7 cycles

13. Which statement about SRAM is FALSE?

A) Uses 1 transistor per cell

B) Faster than DRAM

C) Does not require refreshing

D) More expensive than DRAM

Answer: A) Uses 1 transistor per cell

14. In a direct-mapped cache, memory addresses 0x00 and 0x40 map to the same set. This causes:

A) Capacity misses

B) Ping-pong effect

C) Compulsory misses

D) Spatial locality

Answer: B) Ping-pong effect

15. Which cache level is typically optimized for low hit time?

A) L1

B) L2

C) LLC (Last-Level Cache)

D) Main memory

Answer: A) L1

16. A program with poor temporal locality will likely experience more:

A) Conflict misses

B) Compulsory misses

C) Capacity misses

D) Spatial misses

Answer: C) Capacity misses

17. Which component manages the cache-to-main memory interaction?

A) Operating system

B) Compiler

C) Cache controller hardware

D) CPU scheduler

Answer: C) Cache controller hardware

18. A larger cache block size improves which type of locality?

A) Temporal

B) Spatial

C) Both

D) Neither

Answer: B) Spatial

19. In a 4-way set-associative cache, how many blocks are in each set?

A) 1

B) 2

C) 4

D) Equal to total cache blocks

Answer: C) 4

20. Which parameter does NOT affect AMAT?

A) Hit time

B) Miss rate

C) Clock speed

D) Miss penalty

Answer: C) Clock speed